UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/799,479	03/12/2004	Kenneth Hubbard	CIS03-68(8178)	8394

47654 7590 03/08/2006

DAVID E. HUANG, ESQ.
BAINWOOD HUANG & ASSOCIATES LLC
2 CONNECTOR ROAD
SUITE 2A
WESTBOROUGH, MA 01581

EXAMINER	
KUNZER, BRIAN	
ART UNIT	**PAPER NUMBER**
2814	

DATE MAILED: 03/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/799,479	HUBBARD ET AL.	
	Examiner	Art Unit	
	Brian Kunzer	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *13-28* is/are pending in the application.

4a) Of the above claim(s) ~~*14*~~ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *13 and 15-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Amendment

The amendment filed on December 27, 2005 has been received and entered. Claim 14 has been cancelled and new claims 17-28 have been added.

Claim Objections

1. Claim 25 is objected to because of the following informalities: Claim 25 is dependent on claim 24 and, in turn, dependent on claim 21 and uses the term "electrical contacts" and wherein there is no prior reference of a "secondary electrical contact." Examiner realizes this is a typing error and will read "solder balls" in replace of "electrical contacts" for the purposes of examination. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 13, 15, 18, 20, 21, 24, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jackson (US Patent No. 6,627,822) in view of Byun (US Patent No. 6,736,306).

With respect to claim 13, Jackson teaches, from figs. 1A-1D and 5, the method for manufacturing an area array package comprising:

coupling a grid array of primary electrical contacts (120) to a coupling surface of a substrate (108) within a central portion defined by the substrate, the grid array of primary electrical contacts (120) configured to carry at least data signals between the area array package (108) and a circuit board (101) (see column 4, lines 6-12);

forming the primary electrical contacts as a plurality of solder balls (114), each primary solder ball of the grid array defining a first diameter;

coupling a series of secondary electrical contacts (110) to the coupling surface of the substrate (108) within a peripheral area defined by the coupling surface, the series of secondary electrical contacts configured to carry power signals between the area array package (108) and the circuit board (101) (see column 4, lines 2-6), the series of secondary electrical contacts (110) separate from the grid array.

However, Jackson does not teach forming the series of secondary electrical contacts as a plurality of secondary solder balls, each secondary solder ball of the series defining a second diameter, the second diameter defined by each of the secondary solder balls being greater than the first diameter defined by each of the primary solder balls. Instead, Jackson teaches the use of pins as the secondary electrical contacts.

Byun, drawn to ball grid array design for flip chips, does teach, from figs. 5 and 6, forming the series of secondary electrical contacts as a plurality of secondary solder balls (162), each secondary solder ball of the series defining a second diameter, the second diameter defined by each of the secondary solder balls being greater than the first diameter defined by each of the primary solder balls (160).

Therefore, it would have been obvious to one of ordinary skill in the art, at the time of invention, to create the device of Jackson utilizing the ball grid array of Byun as this would simply replace the pins of Jackson with larger diameter solder balls which still has the same desired effect as described by Jackson to create,

> "an electronic assembly for making power and signal connections between two substrates or between a semiconductor chip, socket or other device and a circuit board or the like that separates the power and signal connections, utilizes the appropriate type of connection and size and shape connection for the function being performed, makes efficient use of available area for making power and signal connections by minimizing the area on the chip or die and on the circuit board needed for making power and signal connections, and may be made efficiently with compatible manufacturing techniques or processes to form both the power and signal connections." (column 2, lines 2-13)

With respect to claim 21, Jackson teaches, from figs. 1A-1D and 5, the method for manufacturing an area array package comprising:

coupling a plurality of primary solder balls (120) to a first set of contact pads disposed on a first surface of a substrate (108), the primary solder balls (120) configured to carry at least data signals between the area array package (108) and a circuit board (101) (see column 4, lines 6-12);

coupling a plurality of secondary electrical contacts (110), the secondary electrical contacts configured to carry power signals between the area array package (108) and the circuit board (101) (see column 4, lines 2-6).

electrically coupling a die to a second surface of the substrate opposing the first surface, the die in electrical communication with the first set of contact pads(see column 2, lines 64-67).

However, Jackson does not teach forming the series of secondary electrical contacts as a plurality of secondary solder balls, each of the secondary solder balls each of the secondary

solder balls having a diameter greater than a diameter of each of the primary solder balls. Instead, Jackson teaches the use of pins as the secondary electrical contacts. In addition, Jackson obviously does not use a second set of contact pads for the pins.

Byun, drawn to ball grid array design for flip chips, does teach, from figs. 5 and 6, coupling a plurality of secondary solder balls (162) to a second set of contact pads (170b) disposed on the first surface of a substrate (120), the second set of contact pads (170b) in electrical communication with at least one conductive plane (120) of the substrate, each of the secondary solder balls (162) having a diameter greater than a diameter of each of the primary solder balls (160).

Therefore, it would have been obvious to one of ordinary skill in the art, at the time of invention, to create the device of Jackson utilizing the contact pads and ball grid array of Byun as this would simply replace the pins of Jackson with larger diameter solder balls which still has the same desired effect as described by Jackson to create,

> "an electronic assembly for making power and signal connections between two substrates or between a semiconductor chip, socket or other device and a circuit board or the like that separates the power and signal connections, utilizes the appropriate type of connection and size and shape connection for the function being performed, makes efficient use of available area for making power and signal connections by minimizing the area on the chip or die and on the circuit board needed for making power and signal connections, and may be made efficiently with compatible manufacturing techniques or processes to form both the power and signal connections." (column 2, lines 2-13)

With respect to claim 15, Jackson, from fig. 5, and Byun, from fig. 8c, teach the method of clam 14 wherein the step of forming the series of secondary electrical contacts (pins of Jackson or second set of solder balls of Byun) comprises:

placing at least two solder balls on a contact pad oriented within the peripheral area defined by the coupling surface, each solder ball defining a first diameter,

heating the at least two solder balls to cause the solder to undergo reflow (see column 5, lines 16-18 of Byun)

forming a secondary solder ball on the contact pad, secondary solder ball of the [series] defining a second diameter, the second diameter defined by the secondary solder ball being greater than the first diameter defined by each of the primary solder balls.

With respect to claim 18, Jackson, combined with Byun, discloses all the limitations except for specifically teaching the method wherein the substrate defines a length of at least approximately 60 mm and a width of at least approximately 60 mm. It would have been obvious to have a substrate with the dimensions of 60mm X 60mm, since such a modification would have involved a mere change in the size of a component. A change in size is generally recognized as being within the level of ordinary skill in the art. In re Rose, 105 USPQ 237 (CCPA 1955).

With respect to claim 20 and 24, both claims comprising similar subject matter, Jackson, combined with Byun, discloses all the limitations except for specifically teaching the method wherein the grid array of primary solder balls is configured in an array pattern of 50 columns having 50 primary solder balls per column. It would have been obvious to have a 50 X 50 grid array, since such a modification would have involved a mere change in the size of a component wherein the number of solder balls could easily be changed with a change in solder ball diameter

or substrate area. A change in size is generally recognized as being within the level of ordinary skill in the art. In re Rose, 105 USPQ 237 (CCPA 1955).

With respect to claim 25, Byun, with Jackson, teaches, from fig. 5, the method wherein the series of secondary solder balls (170) are separate from the grid array (124).

3. Claims 16 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jackson (US Patent No. 6,627,822) and Byun (US Patent No. 6,736,306) as applied to claim 13 and 21 above, and further in view of Barber (US Patent No. 6,600,220).

With respect to claim 16 and 22, both claims comprising similar subject matter, Jackson and Byun teach the method described above.

Jackson and Byun do not specifically teach the coupling of at least one power regulation device to the substrate and in electrical communication with the series of secondary electrical contacts.

Barber, drawn to power distribution in multi-chip modules, teaches, from fig. 1A, coupling a plurality of voltage converters (42) (i.e. a power regulation device) to a substrate (28) in communication with the power supply lines (34) (i.e. series of secondary electrical contacts).

Therefore, it would have been obvious to one of ordinary skill in the art, at the time of invention, to create the device of Jackson coupled with the power regulation scheme of Barber permitting "the multi-chip module (MCM) to receive power at higher voltages than is supported by the high-density thin-film circuit region, decreasing MCM input current magnitudes and reducing noise and energy losses." (abstract of 6,600,220)

4. Claims 17 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jackson (US Patent No. 6,627,822) and Byun (US Patent No. 6,736,306) as applied to claim 13 and 21 above, and further in view of Amir (US Patent No. 6,787,920).

With respect to claim 17 and 23, both claims comprising similar subject matter, Jackson, combined with Byun, discloses all the limitations except for specifically teaching that the method comprises coupling the plurality of secondary solder balls to the substrate at a pitch of at least approximately 5 mm.

However integrated circuit (IC) package designers take into account several design parameters when deciding on the dimension for the pitch (i.e. the interval spacing of the contacts), including the well-known problem of bridging. Bridging occurs during the solder reflow process in which two separate contacts will merge together and short out the circuit because there is a too fine of a pitch. (See column 1, line 66 – column 2, line 8 of Amir.)

Therefore, it would have been obvious to one of ordinary skill in the art, at the time of invention, to have the combined device of Jackson and Byun and have the appropriately sized pitch, such as 5mm, in order to reduce the bridging effect as disclosed by Amir because this specific dimension is the result of finding an optimized parameter for a well known problem which is typically accounted for in all similar devices; and a change in size and discovering an optimum value of a result effective variable is generally recognized as being within the level of ordinary skill in the art. In re Rose, 105 USPQ 237 (CCPA 1955). In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

5. Claims 19, 26 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jackson (US Patent No. 6,627,822) and Byun (US Patent No. 6,736,306) as applied to claim 13 and 21 above, and further in view of Kalidas (US Patent No. 6,396,136).

With respect to claim 19, 26 and 27, all claims comprising similar subject matter, Jackson, combined with Byun, teaches the method as described above.

Jackson and Byun do not specifically teach the method wherein the substrate defines at least one power plane, at least one ground plane, and at least one plated through hole in communication with the at least one power plane and the at least one ground plane, the substrate further comprising a contact pad in electrical communication with the at least one plated through hole and configured to electrically couple with a secondary solder ball.

However, Kalidas, drawn to ball grid array (BGA) package design, discloses, from figs. 4c and 7, a the substrate (703) that defines at least one power plane (703a), at least one ground plane (703b), and at least one plated through hole (703c) in communication with the at least one power plane and the at least one ground plane, the substrate further comprising a contact pad (402b see fig. 4c) in electrical communication with the at least one plated through hole (703c) and configured to electrically couple with a secondary solder ball (708).

Therefore, it would have been obvious to one of ordinary skill in the art, at the time of invention, to have the device of Jackson and Byun featuring a substrate with separate power and ground planes as disclosed by Kalidas, as this is a conventional method to provide power and ground to a chip.

6. Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jackson (US Patent No. 6,627,822) in view of Byun (US Patent No. 6,736,306), Amir (US Patent No. 6,787,920), and Barber (US Patent No. 6,600,220).

Jackson teaches, from figs. 1A-1D and 5, the method for manufacturing an area array package comprising:

coupling a plurality of primary solder balls (120) to a first set of contact pads disposed on a first surface of a substrate (108), the primary solder balls (120) configured to carry at least data signals between the area array package (108) and a circuit board (101) (see column 4, lines 6-12);

coupling a plurality of secondary electrical contacts (110), the secondary electrical contacts configured to carry power signals between the area array package (108) and the circuit board (101) (see column 4, lines 2-6).

electrically coupling a die to a second surface of the substrate opposing the first surface, the die in electrical communication with the first set of contact pads(see column 2, lines 64-67).

However, Jackson does not teach forming the series of secondary electrical contacts as a plurality of secondary solder balls, each of the secondary solder balls each of the secondary solder balls having a diameter greater than a diameter of each of the primary solder balls. Instead, Jackson teaches the use of pins as the secondary electrical contacts. In addition, Jackson obviously does not use a second set of contact pads for the pins.

Byun, drawn to ball grid array design for flip chips, does teach, from figs. 5 and 6, coupling a plurality of secondary solder balls (162) to a second set of contact pads (170b) disposed on the first surface of a substrate (120), the second set of contact pads (170b) in

electrical communication with at least one conductive plane (120) of the substrate, each of the secondary solder balls (162) having a diameter greater than a diameter of each of the primary solder balls (160).

Therefore, it would have been obvious to one of ordinary skill in the art, at the time of invention, to create the device of Jackson utilizing the contact pads and ball grid array of Byun as this would simply replace the pins of Jackson with larger diameter solder balls which still has the same desired effect as described by Jackson to create,

> "an electronic assembly for making power and signal connections between two substrates or between a semiconductor chip, socket or other device and a circuit board or the like that separates the power and signal connections, utilizes the appropriate type of connection and size and shape connection for the function being performed, makes efficient use of available area for making power and signal connections by minimizing the area on the chip or die and on the circuit board needed for making power and signal connections, and may be made efficiently with compatible manufacturing techniques or processes to form both the power and signal connections." (column 2, lines 2-13)

In addition, Jackson, combined with Byun, discloses all the limitations except for specifically teaching the method wherein the grid array of primary solder balls is configured in an array pattern of 50 columns having 50 primary solder balls per column. It would have been obvious to have a 50 X 50 grid array, since such a modification would have involved a mere change in the size of a component wherein the number of solder balls could easily be changed with a change in solder ball diameter or substrate area. A change in size is generally recognized as being within the level of ordinary skill in the art. In re Rose, 105 USPQ 237 (CCPA 1955).

Further, Jackson, combined with Byun, discloses all the limitations except for specifically teaching that the method comprises coupling the plurality of secondary solder balls to the substrate at a pitch of at least approximately 5 mm.

However integrated circuit (IC) package designers take into account several design parameters when deciding on the dimension for the pitch (i.e. the interval spacing of the contacts), including the well-known problem of bridging. Bridging occurs during the solder reflow process in which two separate contacts will merge together and short out the circuit because there is a too fine of a pitch. (See column 1, line 66 – column 2, line 8 of Amir.)

Therefore, it would have been obvious to one of ordinary skill in the art, at the time of invention, to have the combined device of Jackson and Byun and have the appropriately sized pitch, such as 5mm, in order to reduce the bridging effect as disclosed by Amir because this specific dimension is the result of finding an optimized parameter for a well known problem which is typically accounted for in all similar devices; and a change in size and discovering an optimum value of a result effective variable is generally recognized as being within the level of ordinary skill in the art. In re Rose, 105 USPQ 237 (CCPA 1955). In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Finally, Jackson and Byun teach the method described above.

Jackson and Byun do not specifically teach the coupling of at least one power regulation device to the substrate and in electrical communication with the series of secondary electrical contacts.

Barber, drawn to power distribution in multi-chip modules, teaches, from fig. 1A, coupling a plurality of voltage converters (42) (i.e. a power regulation device) to a substrate (28) in communication with the power supply lines (34) (i.e. series of secondary electrical contacts).

Therefore, it would have been obvious to one of ordinary skill in the art, at the time of invention, to create the device of Jackson coupled with the power regulation scheme of Barber

permitting "the multi-chip module (MCM) to receive power at higher voltages than is supported by the high-density thin-film circuit region, decreasing MCM input current magnitudes and reducing noise and energy losses." (abstract of 6,600,220)

Response to Arguments

7. Applicant's arguments filed on December 27, 2005 have been fully considered but they are not persuasive. The Applicant has made two basic arguments which are recited below:

a. "There is no suggestion in either Jackson or Byun to form "secondary electrical contacts configured to carry power signals between the area array package and the circuit board" (e.g., Jackson's pins) as "a plurality of secondary solder balls, each secondary solder ball of the series defining a second diameter, the second diameter defined by each of the secondary solder balls being greater than the first diameter defined by each of the primary solder balls" as claimed by the Applicant."

b. "A combination of Jackson and Byun would result in a device similar to that shown in Jackson's FIG. ID where the solder balls located in proximity to the pins are formed as the connection terminals in Byun such that the solder balls extend over multiple pads. With such a combination, the enhanced solder balls in Jackson would improve the reliability of the solder joint and effectively prevent cracks from forming."

In response to Applicant's argument (a), that there is no suggestion to combine the references, the Examiner recognizes that references cannot be arbitrarily combined and that there must be some reason why one skilled in the art would be motivated to make the proposed combination of primary and secondary references. In re Nomiya, 184 USPQ 607 (CCPA 1975). However, there is no requirement that a motivation to make the modification be expressly articulated. The test for combining references is what the combination of disclosures taken as a whole would suggest to one of ordinary skill in the art. In re McLaughlin, 170 USPQ 209

(CCPA 1971) references are evaluated by what they suggest to one versed in the art, rather than by their specific disclosures. In re Bozek, 163 USPQ 545 (CCPA 1969).

In this case, the dispute lies in whether or not one of ordinary skill in the art, after reading the full disclosures of Jackson and Byun, would be motivated to try using Jackson's device wherein the pins, used as power connectors, are replaced with larger (than the data signal solderballs) solderballs - thereby forming Applicant's claimed invention. Seeing as how both pins and solderballs perform the same basic function (i.e. to provide electrical interconnections in a wide array of microelectronics) and both were well known and utilized to a large extent at the time of the invention, it is the Examiner's position that to create the device of Jackson - with the separate data and power connections - utilizing the ball grid array of Byun would be within the ordinary skill of one in the art. The complete disclosure of Byun and especially Jackson would suggest to one of ordinary skill in the art to attempt such a replacement with a high expectancy of success.

In response to Applicant's argument (b), that with such a combination, the enhanced solder balls in Jackson would improve the reliability of the solder joint and effectively prevent cracks from forming, it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex parte Masham, 2 USPQ 2d 1647 (1987).

In other words, if the combined references provide all the structural limitations of the claim, it doesn't matter if the combined device has an additional desirable end result such as improving the reliability of the solder joint and effectively prevent cracks from forming. In fact,

this would be an additional motivation to combine the two references wherein one would have Jackson's device of fig. 1D and the pins (110) were replaced by solderballs with a larger diameter than the inner solderballs (120) with a similar layout as in Byun and the power and data signals were still separated into the two different interconnections.

Any changes to the original rejections made by the Examiner were initiated by Applicant's amendments and new claims. The majority of the new claims encompassed a new scope and therefore required further searching.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian Kunzer whose telephone number is (571) 272-5054. The examiner can normally be reached on Monday-Friday 8:00-4:30 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

BK
2/28/2006

ANH D. MAI
PRIMARY EXAMINER